

<b>Notice of References Cited</b>		Application/Control No. 09/783,246	Applicant(s)/Patent Under Reexamination HUTTON, MICHAEL D.	
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**U.S. PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Hutton et al., "Equivalence Classes of Clone Circuits for Physical-Design Benchmarking" 1999. pg.VI-428 to VI-431 IEEE.
	V	Hutton et al., "Characterization and Parameterized Random Generation of Digital Circuits" 1996 DAC. pg.94-99.
	W	Hutton et al., "Applications of Clone Circuits to Issue in Physical-Design" 1999. pg.VI-448 to VI-451 IEEE.
	X	Wilton, S.J.E., "Heterogeneous Technology Mapping for Area Reduction in FPGA's with Embedded Memory Arrays" 2000. IEEE pg. 56-68.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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	U	Hutton et al., "Timing-Driven Placement for Hierarchical Programmable Logic Devices" 2001. pg.3-11 FPGA 2001.
	V	Hutton et al., "Characterization and Parameterized Generation of Synthetic Combination Benchmark Circuits" 1998. pg. 985-996 IEEE.
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